ABSTRACT OF THE DISCLOSURE

A dummy cell (reference electric potential generating circuit) DC has a paraelectric capacitor DCC1 and a ferro-electric capacitor DCC2. One end of the paraelectric capacitor DCC1 and one end of the ferro-electric capacitor DCC2 are commonly connected to a node N1. A dummy plate electric potential DPL1 is supplied to the other end of the paraelectric capacitor DCC1, and a dummy plate electric potential DPL2 is supplied to the other end of the ferro-electric capacitor DCC2. When data of a memory cell MC is read at a bit line (selective bit line) BL1, a reference electric potential is supplied to a bit line (reference bit line) BL2 from the dummy cell DC.